In the Claims

1. (Previously presented) A semiconductor processing method of forming transistors comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different;

forming a gate line over respective active areas to provide individual transistors, the transistors corresponding to the active areas having the different widths having different threshold voltages, wherein a transistor corresponding to an active area having a smaller of the different widths has a lower of the different threshold voltages; and

wherein the active areas having the different widths each comprise a width of less than one micron.

2. (Previously presented) The semiconductor processing method of claim 1 further comprising providing the different threshold voltages without using a separate channel implant for the transistors.

3. (Previously presented) The semiconductor processing method of claim 1, wherein all the individual transistors formed using the substrate correspond to active areas having widths that are each less than one micron.

4. (Original) The semiconductor processing method of claim 1, wherein the different threshold voltages are each less than 2 volts.

5. (Original) The semiconductor processing method of claim 1, wherein the different threshold voltages are each less than 1 volt.

6. (Original) The semiconductor processing method of claim 1, wherein the two different widths are each less than one micron, and the different threshold voltages are each less than 2 volts.

7. (Original) The semiconductor processing method of claim 1, wherein the two different widths are each less than one micron, and the different threshold voltages are each less than 1 volt.

Claims 8-50 (Canceled).

51. (Previously presented) The method of claim 1, wherein forming individual transistors comprises forming at least one active area of one of the transistors to have a width greater than one micron.

52. (Previously presented) The method of claim 1, wherein forming individual transistors comprises forming three individual transistors, a first of the three having a first threshold voltage, a second of the three having a second threshold voltage greater than the first threshold voltage and a third of the three having a third threshold voltage greater than the second threshold voltage.

53. (Previously presented) The method of claim 1, wherein forming individual transistors comprises forming at least three individual transistors, a first of the three having a first threshold voltage, a second of the three having a second threshold voltage greater than the first threshold voltage and a third of the three having a third threshold voltage greater than the second threshold voltage, the three individual transistors being configured to be coupled in parallel.

54. (Previously presented) A semiconductor processing method of forming transistors comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths over the substrate, at least two of the widths being different, at least one of the plurality of active areas having a width less than one micron;

forming a gate line over respective active areas to provide individual transistors having different threshold voltages, the transistors being provided with the different threshold voltages without using separate channel implants for different ones of the transistors;

performing a plurality of channel implants common to the transistors to provide the different threshold voltages; and

wherein a transistor with a lower one of the threshold voltages corresponds to the active area having a smaller one of the widths.

55. (Previously presented) The method of claim 54 further comprising forming a transistor having a higher one of the threshold voltages to have an active area width greater than one micron.

56. (Previously presented) The method of claim 54 further comprising forming a transistor having one of a higher of the threshold voltages to have an active area width less than one micron.

Claim 57 (Canceled).

58. (Previously presented) The method of claim 54, wherein the forming of the gate line comprises forming a common gate line over the plurality of active areas.

59. (Previously presented) The method of claim 54, wherein forming the gate line comprises forming a common gate line over the plurality of active areas, the transistors being formed in a parallel configuration.

60. (Previously presented) The method of claim 54, wherein the different threshold voltages are each less than 1 volt.

61. (Previously presented) The method of claim 54, wherein the at least two of the different widths are each less than one micron, and the different threshold voltages are all less than 2 volts.

62. (Previously presented) The method of claim 54, wherein at least two of the different widths are each less than one micron, and the different threshold voltages are all less than 1 volt.

63. (Previously presented) A semiconductor processing method of forming transistors comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron, at least two of the widths being different; and

forming a gate line over respective active areas to provide individual transistors, the transistors corresponding to the active areas having the different widths having different threshold voltages without using a separate channel implant for the transistors, wherein the different threshold voltages are each less than 2 volts.

64. (Previously presented) The semiconductor processing method of claim 63, wherein the at least two different widths are less than one micron.

65. (Previously presented) The semiconductor processing method of claim 63, wherein the different threshold voltages are each less than 1 volt.

66. (Previously presented) The semiconductor processing method of claim 63, wherein the at least two different widths are less than one micron, and the different threshold voltages are less than 1 volt.

67. (Previously presented) A semiconductor processing method of forming transistors comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas having widths over the substrate, at least two of the widths being different, at least one of the plurality of active areas having a width less than one micron;

forming a gate line over respective active areas to provide individual transistors having different threshold voltages, the transistors being provided with the different threshold voltages without using separate channel implants, wherein forming the gate line comprises forming a common gate line over the plurality of active areas, the transistors being formed in an electrically parallel configuration; and

wherein a transistor with a lower one of the threshold voltages corresponds to the active area having a smaller one of the widths.

68. (Previously presented) The method of claim 67 further comprising forming a transistor having a higher one of the threshold voltages to have an active area width greater than one micron.

69. (Previously presented) The method of claim 67 further comprising forming a transistor having one of a higher of the threshold voltages to have an active area width less than one micron.

70. (Previously presented) The method of claim 67 further comprising conducting only one common channel implant for the plurality of transistors.

71. (Previously presented) The method of claim 67, wherein the forming of the gate line comprises forming a common gate line over the plurality of active areas.

72. (Previously presented) The method of claim 67, wherein the different threshold voltages are each less than 1 volt.

73. (Previously presented) The method of claim 67, wherein the at least two of the different widths are each less than one micron, and the different threshold voltages are all less than 2 volts.

74. (Previously presented) The method of claim 67, wherein forming individual transistors comprises forming at least three individual transistors, a first of the three having a first threshold voltage, a second of the three having a second threshold voltage greater than the first threshold voltage and a third of the three having a third threshold voltage greater than the second threshold voltage, the three individual transistors being configured to be coupled in parallel.

Claims 75-84 (Canceled).

85. (Previously presented) The method of claim 53, wherein respective ones of power terminals of the three individual transistors are commonly coupled with one another.

86. (Previously presented) The semiconductor processing method of claim 63, wherein the transistor having a higher of the different threshold voltages comprises a larger of the different widths.

87. (Previously presented) The method of claim 1, wherein two of the transistors having different threshold voltages are formed immediately adjacent to one another.

88. (Previously presented) The method of claim 1 further comprising performing a plurality of channel implants common to the transistors to provide the different threshold voltages.

89. (Previously presented) The method of claim 88, wherein the channel implants are the only channel implants in the substrate for the transistors.

90. (Previously presented) The method of claim 54, wherein the channel implants are the only channel implants in the substrate for the transistors.

91. (Previously presented) The method of claim 54, wherein two of the transistors having different threshold voltages are formed immediately adjacent to one another.

92. (Previously presented) The method of claim 54, wherein the different threshold voltages of the transistors are provided using the same channel implants common to the transistors.

93. (Previously presented) The method of claim 54, wherein the active areas having the different widths each comprise a width of less than one micron.

94. (Previously presented) The method of claim 64, wherein the active areas having the different widths each comprise a width of less than one micron.

95. (Previously presented) The method of claim 67, wherein the active areas having the different widths each comprise a width of less than one micron.

96. (Previously presented) The method of claim 67, wherein at least one transistor comprises a switching transistor.

97. (Previously presented) The method of claim 67, wherein at least one transistor comprises a pass transistor.

98. (Previously presented) The method of claim 67, wherein the individual transistors are configured in DRAM circuitry which is configured to store data.

99. (Previously presented) The method of claim 67, wherein the individual transistors are configured in precharge circuitry.